

TIME SYNCHRONIZATION FOR PASSIVE SURVEILLANCE SYSTEMS

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Abstract—Passive Surveillance Systems (PSS) are emitter location systems based on electromagnetic signals emitted by radars. The basic principle of operation is by Differential Time Of Arrival (D-TOA) of signals at geographically distributed sensors. Time synchronization of the sensors is the most critical aspect for PSS, as the accuracy of TOA and thereby emitter location accuracy is dependent on it. The present paper discusses the time synchronization based on Common View GPS, its utilization in PSS and the accuracies achieved.

Keywords—Passive Surveillance Systems, Synchronization DTOA, ESM

I. INTRODUCTION

A fast and accurate location fixing technique is very important in Electronic Warfare scenario. Different techniques like TDOA/AOA/FDOA are employed for accurate measurement of location of the emitter. Localization by time difference of arrival (TDOA) is a passive location estimation method that utilizes the differences between the arrival times of pulses transmitted by an emitter without prior knowledge of pulse transmit times. The time differences are measured at multiple receivers at known locations, and subsequently used for computing a location estimate of the unknown emitter. To detect and locate threat accurately, precise time synchronization between signal receiving stations is required which is the core technology for TDOA based emitter location systems.

The technique for achieving time synchronization depends on the distance between the sensors. If the sensors are not too far away, i.e. of the order of few hundred meters, a dedicated cable can be used. This allows much better control between the sensors and helps in achieving a much better synchronization performance.

Time Synchronization for distributed receivers, where a wired link cannot be provided, can be achieved by two methods.

1. Common system clock
2. Distributed system clock

In distributed system clock, the 1PPS signal is generated at each of the signal receiver module. In common system clock, 1PPS signal can be generated at one of the receivers and it is transferred to the other signal receiver modules. Highly stable Atomic clocks are used for generation of the common clocks and the same is transmitted to all the sensors. In the case of

distributed clock systems, a 1PPS signal is generated at each of the receivers and the clocks are corrected to ensure that they are synchronized against each other to the required accuracy. An optimum solution to this problem is to use GPS receiver based timing generation system.

II. TIME SYNCHRONIZATION REQUIREMENTS

The main aim of the Time Synchronization System is to provide a common clock across all the geographically distributed sensors so that the time of arrival of the signal can be measured accurately. The accuracy of the synchronization is critical since the accuracy of TOA and thereby emitter location accuracy is directly dependent on it. The commercially available Timing GPS receivers provide an accuracy of ± 50 ns, which is not sufficient for high accuracy location fix systems.

Two way time transfer based time synchronization systems are well established for time transfer to the order of sub nanosecond. But they require dedicated satellite bandwidth, and are hardware intensive.

One of the main system requirements against which the time synchronisation was developed was that the realized system should be of small size, low cost and with very less power consumption and should be capable of supporting realtime location fix requirements of Passive Surveillance Systems with a required emitter location Circular Error Probability (CEP) of 500m. Also the data link requirements between sensor stations should be minimal. Common View GPS (CVGPS) based time synchronization has been chosen for development since it meets all the above requirements.

To meet the futuristic requirements of time synchronization for various surveillance systems, DLRL and CSIR-NPL have successfully collaborated towards the development of the indigenous CVGPS system to achieve a time synchronization accuracy of a few nanoseconds. All required software has been indigenously developed by CSIR-NPL and testing done at NPL against their UTC-NPLI.

A. Theory of CVGPS

CVGPS involves receiving signals from a GPS satellite S at two receiving sites A and B, each containing a GPS receiver and a local clock (Fig 1). The stations A and B each compare the received GPS signal to their local clock. Thus, the site A

compares the GPS signal received over the path d_{SA} to the local clock yielding the measurement of clocks A-S. Likewise, the site B receives GPS over the path d_{SB} and measures clock B-S. The difference between these two measurements is an estimate of (clock A-clock B) as given in the basic equation for CVGPS measurement.

$$\text{clock (A-S)} - \text{clock (B-S)} = (\text{clock A} - \text{clock B}) + (e_{SA} - e_{SB}) \quad \text{-----(1)}$$

Here e_{SA} and e_{SB} are the errors due to the signal propagation in the atmosphere. If the two clocks are not located very far away from each other (i.e. located within a few tens of kilometers), as the case is with passive surveillance systems, it can be assumed that e_{SA} and e_{SB} are equal and difference is zero, since the GPS signal passes through almost the same path. In such condition (clock (A-S)-clock (B-S)) gives the difference between the two clocks which can be used to correct the two clocks against each other.

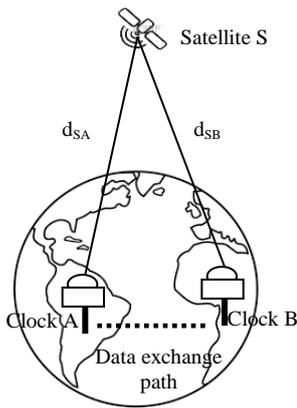


Fig 1. Common View GPS principle

B. Implementation of CVGPS

The block schematic of the CVGPS system is shown in Fig 2. It consists of a designated Master station and several slave stations connected to the master by a data exchange channel. The hardware at the master and the slave stations are, in principle, identical except that, at a designated master station one could use a more stable and accurate Cs clock for better long term stability. The hardware at each site comprises a multichannel GPS timing receiver (C/A code, L1-band GPS engines such as Trimble Resolution-T) and a Time Interval counter, which measures the difference between the received GPS signal and the local clock based on a Rb frequency standard. The Time Interval (TI) data is logged by a single board PC in CGGTTS (CCTF Group on GNSS Time Transfer Standards) format. In order to get the TI measurement

corresponding to individual satellites and remove the so-called quantization errors of the 1pps output, additional information needs to be downloaded from the GPS engine by the PC. The laboratory realization is as given in Fig 3.

The raw measurements, averaged over 15 min satellite passes and stored as CGGTTS files, are transmitted to the Master station at regular intervals of few hours. Following each data transfer, the processor at the Master station runs an application that uses the CGGTTS files of the master and slave – it aligns and differences the data of individual satellite tracks and discards the data that are not common view at both stations. In our case since the station separation is very small most of the satellite tracks are in common view. This difference file is the CVGPS data, and as explained in Eq. 1, yields the Time Difference TD between the Clocks at the Master and the Slave. Our goal is to make TD=0. This can be accomplished by a PID control loop feedback mechanism in which we use TD as a process variable and steer the frequency of the Rb clock in order to get TD to approach 0. The feedback on the required frequency steering is sent back to the slave station on the data channel. The demand on the data channel is not very heavy. It is typically a few hundred kB every few hours for the data transfer from the slave to the master and a few kB for the frequency steering information from the Master to the Slave.

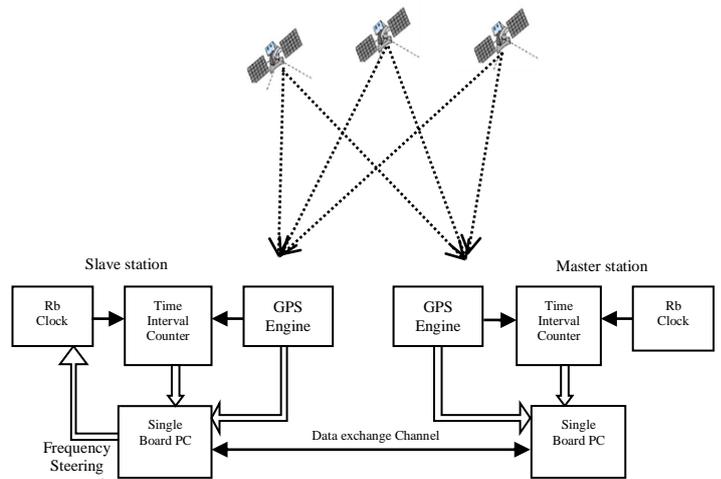


Fig 2. Implementation of CVGPS

C. Testing:

The synchronization accuracy between two CVGPS modules has been tested by co-located operation and measurements. The block diagram of the experimental set up for lab testing has been shown in fig 3.

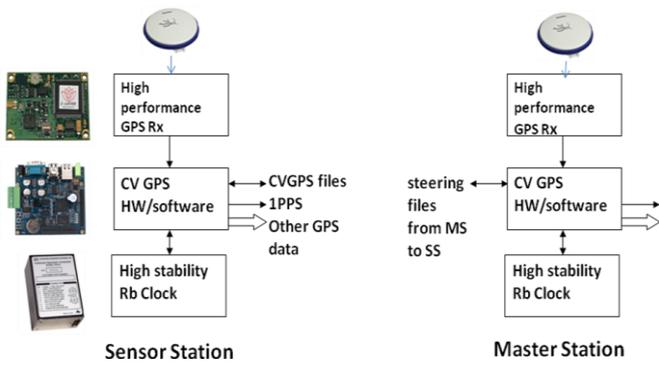


Fig 3. Block diagram of experimental setup for Time synchronization system

An inbuilt TIC of the Rb frequency standard compares 1PPS output from one of the GPS receiver with one of the Rb atomic clock, which is considered as a master clock and that data is stored in a Single Board Computer (SBC). Other Rb clocks are considered as Slaves and the 1PPS output of the other slave clocks are also compared with other GPS receivers stored in separate SBC. All the Rb clocks are interconnected through a communication channel and the Master clock steers all the Slave clocks. A common clock (UTC-NPLI) is also used for comparing the 1 PPS output for both Master and Slave clocks which give options for direct comparison between the master and slave clocks.

The synchronization has been tested between three Rubidium Clocks designated as PRS1 (Rb1), PRS2 (Rb2) and PRS3(Rb3). (Model No. PRS10 of Stanford Research Systems). Fig 4(a) shows Inter comparison data for time synchronisation for one Rubidium (Rb1) against UTC-NPLI with calculated jitter (σ) \approx 2.0 ns.

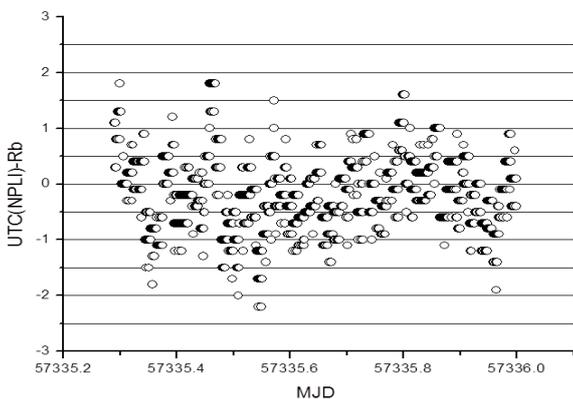


Fig 4(a). Achieved Synchronisation (in ns) between Rubidium and UTC NPLI

Fig 4(b) shows extended test results for the Rubidium against UTC-NPLI with calculated jitter (σ) \approx 2.0 ns.

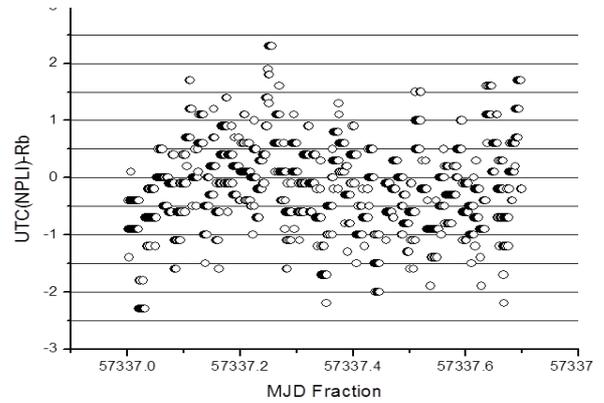


Fig 4(b). Achieved Synchronisation (in ns) between Rubidium and UTC NPLI (extended testing)

The critical performance of time synchronization between two Rubidium clocks, where one Rubidium clock acts as the Master clock has also been carried out. The results are given in Fig 5(a) to Fig 5(c).

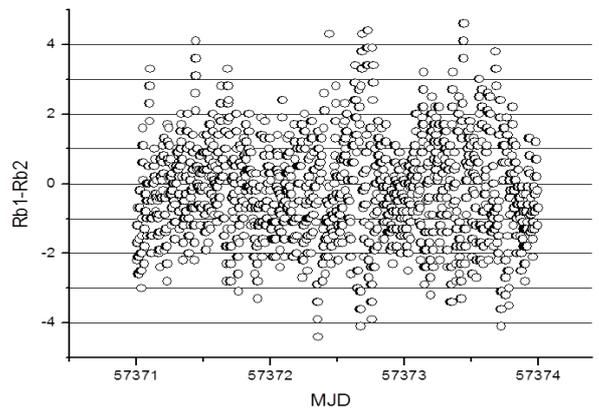


Fig 5(a) Achieved Synchronisation(in ns)between PRS1, PRS2

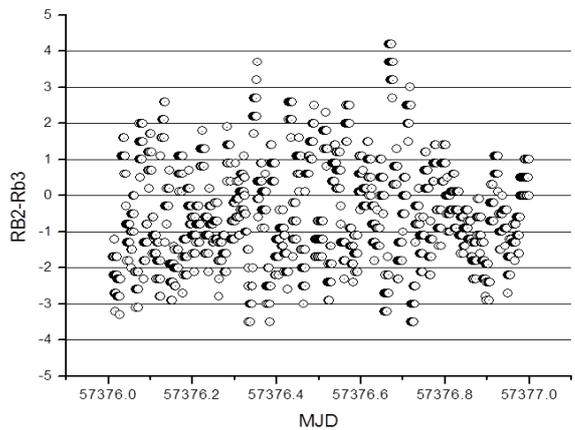


Fig 5(b) Achieved Synchronisation (in ns)between PRS2, PRS3

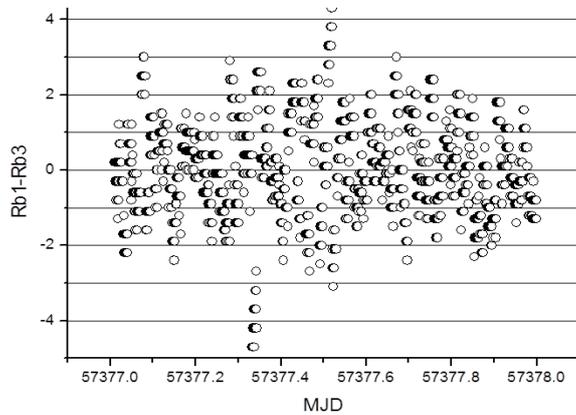


Fig 5(c) Achieved Synchronization (in ns) between PRS1, PRS3

In the Fig 5(a), the Rb1 has been considered as the Master clock and Rb2 is designated as Slave clock. The deviation of Slave against Master is plotted. Similarly in Fig 5(b), deviation of Slave (Rb3) against Master (Rb2) is plotted. In Fig 5(c), deviation of Slave (Rb3) against Master (Rb1) is plotted.

The results show a time synchronization accuracy of 3 ns (rms) meeting the requirement of Passive Surveillance systems.

III. CONCLUSIONS

A light weight, low cost, low power consuming time synchronization system for geographically distributed Passive Surveillance Systems has been successfully designed and developed using Common View GPS. A synchronization accuracy of ~ 2 ns rms has been achieved, when one Rubidium Clock is tested against a stable UTC-NPLI reference and ~ 3 ns rms when the Rubidium Clocks are tested against each other. This accuracy meets the requirements of Location Fix systems based on multilateration to achieve a desired accuracy of 500m CEP.

This technique is very versatile and has the potential for synchronization of not only stationary sensors but also moving sensors. Experimentation for implementation of the same is currently under progress.

Acknowledgments

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